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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/530,549	06/30/2000	ALBRECHT MAYER	P00.0665	8828

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EXAMINER

GARCIA OTERO, EDUARDO

ART UNIT	PAPER NUMBER
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2123

DATE MAILED: 12/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/530,549

Applicant(s)

MAYER, ALBRECHT

Examiner

Eduardo Garcia-Otero

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 October 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 and 13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 and 13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION: Final Action

Introduction

1. Title is: METHOD AND DEVICE FOR SYSTEM SIMULATION OF MICROCONTROLLERS/MICROPROCESSORS AND CORRESPONDING PERIPHERAL MODULES.
2. First named inventor is: MAYER.
3. This action is in response to Applicant's Amendment received 10/24/03: amending claim 9, canceling claim 12, adding claim 13.
4. Claims 7-11, and 13 are pending, and are rejected.
5. Said amendment is accepted without objection, it does not introduce new matter.
6. This Application is a 371 of PCT/DE99/02778 09/02/1999.

Index of Prior Art

7. **Bhandari** refers to US Patent 5,663,900.

Applicant Remarks

8. Remarks, page 6-8. The prior 35 USC 101 and 35 USC 112 rejections are withdrawn due to Applicant's amendments, cancellations, and assertions. However, a new 35 USC 101 rejection is made for new claim 13.
9. TWO MODES. Applicant's specification discusses at least two distinct modes for controlling simulated clock timing during simulations. In the first mode, "precise clock cycle, all modules are always cosimulated" at specification page 1 line 23, and "unified processor clock" at page 2 line 2.
10. In the second mode, "the two systems are largely decoupled... clocks of the components run independently and to synchronize them only at those points at which an interaction between the systems occurs, and only for the strictly necessary number of cycles" at page 2 line 14.
11. Applicant's claimed invention appears to be an intended acceleration of the second mode, per specification page 3 line 5.
12. TERMINOLOGY. Remarks page 8-11. Applicant raises several interpretation issues.
13. MARKER. Applicant cites the Merriam-Webster CD dictionary v 2.5 (c) 2000 as defining "**marker**" as "2.f: something (as a person, flag, stake, ship) posted at a point to indicate

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a position (as of a military unit, on obstacle)". Technical dictionaries are generally preferred when words are used as a technical field such as computer programming, see below.

14. Microsoft Computer Dictionary Fourth Edition, (c) 1999 defines "**marker**" as "n. 1. Part of a data communications signal that enables the communications equipment to recognize the structure of the message. Examples are the start and stop bits that frame a byte in asynchronous serial communications. 2. A symbol that indicates a particular location on a display." Also defines "**mark**" as "n. 1. In applications and data storage, a symbol or other device used to distinguish one item from others like it. 2. In digital transmission, the state of a communications line (positive or negative corresponding to binary 1. In asynchronous serial communications, a mark condition is the continuous transmission of binary 1s to indicate when the line is idle (not carrying information). In asynchronous error checking..."

15. The McGraw-Hill Dictionary of Scientific and Technical Terms, 4th Edition, 1989 defines "mark" as "[COMPUTER SCI] A distinguishing feature used to signal some particular location or condition." This appears to be the most relevant definition. (The 6th Edition has the same definition.) However, the Applicant appears to use the "markers" to do more complex tasks such as turning off the simulation clock, possibly through transferring control, and possibly transferring control through software interrupts.

16. **Note that Applicant's exemplifying embodiment at page 5 line 16 and line 21 uses "The opcode afh, which is not ordinarily used" as "markers", and these markers appear to function as software interrupts, or as unconditional jumps, or possibly even as subroutine calls.**

17. INTERRUPT. Microsoft Computer Dictionary defines "**interrupt**" as "n. A signal from a device to a computer's processor requesting attention from the processor. When the processor receives an interrupt, it suspends its current operations, saves the status of its work, and transfers control to a special routine known as an interrupt handler, which contains the instructions for dealing with the particular situation that caused the interrupt. Interrupts can be generated by various hardware devices to request service or report problems, or by the processor itself in response to program errors or requests for operating system services. Interrupts are the processor's way of communicating with the other elements that make up a computer system. A hierarchy of interrupt priorities determines which interrupt request will be handled first if more

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than one request is made. A program can temporarily disable some interrupts if it needs the full attention of the processor to complete a particular task. See also exception, external interrupt, hardware interrupt, internal interrupt, software interrupt.”

18. Also Microsoft Computer Dictionary defines “**software interrupt**” as “n. A program-generated interrupt that stops current processing in order to request a service provided by an interrupt handler (a separate set of instructions designed to perform the task required). Also called trap.”

19. Note that Applicant’s exemplifying embodiment at page 5 line 16 and line 21 uses “The opcode afh, which is not ordinarily used” as “markers”, and **these markers appear to function as software interrupts, or as unconditional jumps, or possibly even as subroutine calls.**

20. STANDARED CONTROL TRANSFER TECHNIQUES. Remarks page 9. Applicant unpersuasively asserts “marker” is not disclosed by Bhandari at column 2 line 7 “software program... single step... interrupt”. First, note that Bhandari fully states “**control simulation operations, (e.g. start, single step, monitor, or interrupt.)**”. Thus, one of ordinary skill in the art would interpret Bhandari as including “software interrupt” defined above, as well as other well known standard control techniques. For example, standard control transfer instructions include: A) jumps (unconditional jump instructions, call instructions, and return instructions), and B) interrupts (which can be inserted by the programmer, or caused by hardware events, or caused by software events such as input/output), and C) conditional control transfer (commonly referred to as a conditional branch). Applicant’s “marker” is not conditional. See also Bhandari column 6 line 28 “module coordination... functional cooperation with the simulator”.

21. Applicant also unpersuasively asserts that “interrupt” is a verb, and “verbs are not tangible things that could be “removed” [after simulation is completed]”. Note that “interrupt” and “software interrupt” are nouns according to the Microsoft Computer Dictionary, although “interrupt” can also be used as a verb in either a technical or non-technical sense. Further note that software interrupts may be inserted and removed as desired.

22. Similarly, Bhandari’s “start” can also be used as a noun, in the sense of an instruction that starts, similar to an interrupt that interrupts.

23. Remarks page 11, regarding claim 9. Applicant asserts that in “Bhandari, it is the program codes of the software of the control program that is executed” and unpersuasively

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distinguishes Bhandari from claim 9 “sequence steps correspond to program codes of the modules to be simulated”.

24. Note that Applicant’s exemplifying embodiment at page 5 line 16 and line 21 uses “The opcode afh, which is not ordinarily used” to control synchronicity with the other modules. Specifically, specification page 5 line 25 states “The program code is directly processed between the markers without the simulation model requiring clock pulse edges.” **Thus, Applicant’s “markers” appear to interact (as software interrupts, or jumps, or perhaps calling a subroutine) with a control program which enforces synchronicity or allows non-synchronicity (toggles synchronicity) with the other modules.**

25. Also see page 7 line 22 which states that “the clocks of all subcomponent” are “basically rigidly coupled and run synchronously. The sole exception is what is known as lightspeed mode, in which the clock of the [simulated] hardware components is quiescent though the software still runs on the CPU. Before the software accesses the [simulated] hardware, the lightspeed mode must be explicitly exited, which is triggered by special markers that are otherwise not present in the program.” Thus, the “markers” are “triggering” substantial changes in the timing relationships between the modules. See also Bhandari column 6 line 28 “module coordination... functional cooperation with the simulator”.

Claim Rejections - 35 USC § 101-statutory subject matter

26. 35 U.S.C. 101 reads as follows: Whoever invents or discovers any new and useful **process, machine, manufacture, or composition of matter**, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

27. **Claim 13 is rejected under 35 U.S.C. 101** because the claimed invention is directed to non-statutory subject matter.

28. Claim 13 preamble states “An apparatus for carrying system simulation, comprising:”. Thus, claim 13 appears to intended as a “machine” (or apparatus) according to the statutory categories of 35 USC 101.

29. However, the claim 13 limitations include “a simulated microcontroller or microprocessor module...” which appears to be claiming a software module.

30. Another limitation states “a first sequence of steps comprising...”, which appears to be a process step category according to 35 USC 101.

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31. Another limitation states “system states”, and it is not clear what statutory category this relates to, but appears to refer to “system simulation” from the preamble.

32. See MPEP 2173.05(p)(II), which states:

A single claim which claims both an apparatus and the method steps of using the apparatus is indefinite under 35 U.S.C. 112, second paragraph. In *Ex parte Lyell*, 17 USPQ2d 1548 (Bd. Pat. App. & Inter. 1990), a claim directed to an automatic transmission workstand and the method steps of using it was held to be ambiguous and properly rejected under 35 U.S.C. 112, second paragraph. Such claims should also be rejected under 35 U.S.C. 101 based on the theory that the claim is directed to neither a “process” nor a “machine,” but rather embraces or overlaps two different statutory classes of invention set forth in 35 U.S.C. 101 which is drafted so as to set forth the statutory classes of invention in the alternative only. *Id.* at 1551.

33. Also see MPEP 2106 regarding computer related inventions.

34. Note that “software” is generally not patentable as such, but must be claimed as process steps, or as machine, or as manufacture. For example, software may be claimed as machine or [article of] manufacture by stating “a computer readable media containing instructions, which when executed, cause the following steps to be performed”.

35. In the Applicant’s claimed invention, it is particularly critical to identify whether the various components are being simulated by hardware or by software.

Claim Interpretation

36. **The claim language is interpreted in light of the specification.** Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

37. Claim 7 states “signal patterns”, and “markers”.

38. **“Signal patterns”** is interpreted as including “sequences of code”.

39. **“Markers”** is interpreted as “code or sequences of code that are not usually used in program code, used to signal some particular location or condition”. Also see discussion above. The “markers” appear to be used to perform (“trigger”) complex tasks, such as interrupting or jumping or perhaps calling subroutines.

35 USC § 102: filed after 11/29/00, or vol. pub. under 35 USD 122(b)

40. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless – (e) the invention was described in- (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed

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under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

41. **Claims 7-11 are rejected under 35 U.S.C. 102(e).**

42. Claim 7 is rejected under 35 U.S.C. 102(e) as being anticipated by Bhandari.

43. Claim 7 is an independent claim with 5 limitations, labeled A-E by the Examiner for clarity.

44. **A-in a first sequence of steps, simulating said microcontroller/microprocessor and said peripheral modules with predetermined signal patterns** is disclosed by Bhandari at Abstract “various models are simulated and interfaced to certain target systems, logic analyzers, modeler, functional testers, emulators, hardware accelerators, hardware modelers, or other simulators”. More specifically, “first sequence of steps” is disclosed at column 2 line 8 “software program is used to control simulation operations”, and “microcontroller/microprocessor” is disclosed by “integrated circuits” at column 1 line 16, and “peripheral modules” is disclosed at column 1 line 62 “external systems may include other simulators... which may cooperate functionally with the primary simulation facility”.

45. **B-said first sequence of steps having markers inserted therein** is disclosed by Bhandari at column 2 line 7 “software program is used to control simulation operation... single step, monitor, or interrupt”, and column 6 line 28 “module coordination... functional cooperation with the simulator”.

46. **C-in a second sequence of steps, interrogating and evaluating states of said system brought about by said simulation** is disclosed by Bhandari column 1 line 33 “generate verifiable, imitated functional or logical output signals in response to stimuli applied to the model”, and column 2 line 7 “software program... monitor”. Note that Bhandari “verifiable” implies verifying by interrogating and evaluating the output signals of the model to verify the functional or logical behavior of the model. Further note that Bhandari “software program... monitor” also implies verifying by interrogating and evaluating the output signals. And Bhandari column 6 line 28 “module coordination... functional cooperation with the simulator”.

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47. **D-interrupting first sequence of steps for executing said second sequence of steps as dictated by said markers inserted into said first sequence** is disclosed by Bhandari at column 2 line 7 “software program is used to control simulation operation... single step, monitor, or interrupt” and column 6 line 28 “module coordination... functional cooperation with the simulator”.

48. **E-said second sequence of steps being executed in an accelerated operational mode that is adapted to said evaluation** is disclosed by Bhandari at column 2 line 7 “software program is used to control simulation operation... single step, monitor, or interrupt”. Note that single step and interrupt will each freeze the simulated time after executing the single step or interrupt. Thus, simulated time does not elapse during monitoring or analysis, after executing single step or interrupt. Note specification page 3 line 17 states “in the accelerated code mode [or accelerated operational mode] “simulated” time does not elapse”. And Bhandari at column 4 line 21 “asynchronous operation”, and column 6 line 28 “module coordination... functional cooperation with the simulator”.

49. Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Bhandari.

50. Claim 8 depends from claim 7, with one additional limitation.

51. **“said first sequence of steps provides a clock-cycle-based simulation of said microcontroller/microprocessor and of said peripheral modules”** is disclosed by Bhandari at column 4 line 13 “second simulation tool may be synchronized with the primary simulator”.

52. Claim 9 (currently amended) is rejected under 35 U.S.C. 102(e) as being anticipated by Bhandari.

53. Claim 9 (currently amended) depends from claim 7, with one additional limitation.

54. **“said first sequence of steps is a series of consecutive program codes corresponding to program codes of at least one of the modules to be simulated”** is disclosed by Bhandari at column 2 line 7 “software program is used to control simulation operation... single step, monitor, or interrupt”.

55. Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by Bhandari.

56. Claim 10 depends from claim 9, with one additional limitation.

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57. **“markers are formed by one of opcodes or opcode sequences that are not usually used in said program code”** is disclosed by Bhandari at column 2 line 7 “software program is used to control simulation operation... single step, monitor, or interrupt”.

58. Claim 11 is rejected under 35 U.S.C. 102(e) as being anticipated by Bhandari.

59. Claim 11 depends from claim 7, with one additional limitation.

60. **“peripheral modules that were specified during said second sequence of steps are functionally cosimulated”** is disclosed by Bhandari at column 1 line 62 “external systems may include other simulators... which may cooperate functionally with the primary simulation facility”, and at column 4 line 13 “synchronized”, and Bhandari column 6 line 28 “module coordination... functional cooperation with the simulator”.

Conclusion

61. All claims are rejected. Note that Bhandari could also serve as 102(a) type prior art.

Response to Amendments or new IDS-FINAL OFFICE ACTION

62. Applicant's amendments or new IDS necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

63. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 7:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for this

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group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * * *



KEVIN J. TESLA
SUPERVISORY
PATENT EXAMINER